PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-077218
(43)Date of publication of application : 14.03.2000

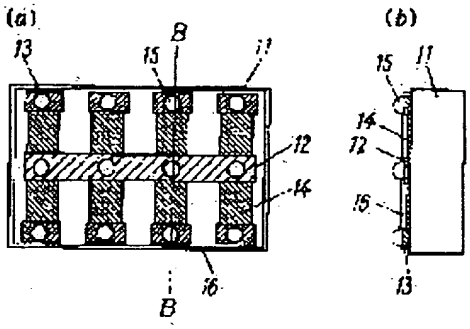
(51)Int.Cl. H01C 13/02

(21)Application number : 10-246781
(22)Date of filing : 01.09.1998

(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : KINOSHITA TAIJI
SHIBUYA NAOKI
HOSHITOKU SEIJI

(54) RESISTOR NETWORK CHIP

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a resistor network chip for making it difficult for any part or a set into which a resistor network chip is integrated to malfunction, even when it is used in a high frequency circuit.
SOLUTION: This resistor network chip is constituted of a rectangular insulating substrate 11, plural individual electrodes 13 provided at the edge part of the insulating substrate 11, plural resistance elements 14 provided so as to be connected with the individual electrodes 13, a common electrode 12 provided to be electrically connected with the resistance elements 14, and bumps 15 provided in the neighborhood of the both edges of the common electrode 12 and at the other parts. It is desired that the bump electrodes 15 be provided at all junctions of the common electrode 12 and the resistance elements 14.



LEGAL STATUS

[Date of request for examination] 10.03.2005

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The chip form resister network which consists of a rectangle-like insulating substrate, two or more individual electrodes prepared in the edge of this insulating substrate, two or more resistance elements prepared so that it might be joined to said individual electrode, a common electrode prepared so that it might be joined to said resistance element and electric target, and a bump electrode prepared in parts other than near the ends near the ends of this common electrode.
[Claim 2] The chip form resister network according to claim 1 which prepared the bump electrode in all the junctions of a common electrode and a resistance element.
[Claim 3] The chip form resister network which becomes the both ends of a rectangle-like insulating substrate and this insulating substrate from two or more resistance elements prepared so that two individual electrodes which face the individual electrode of same number **********, respectively might be joined, respectively, the common electrode prepared so that it might be joined to said all resistance elements and electric targets ranging over all these resistance elements, and the bump electrode prepared at all the junctions of said common electrode and resistance element.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the chip form resister network which has a common electrode.
[0002]
[Description of the Prior Art] What was indicated by JP,5-33517,A is known as this conventional kind of a chip form resister network.
[0003] Hereafter, the conventional chip form resister network is explained, referring to a drawing.

[0004] The said [can set drawing 4 (a) to the plan of the conventional chip form resister network, and / drawing 4 / (b)] sectional view between A-A of drawing 4 (a) and drawing 4 (c) are drawings showing this equal circuit.
[0005] in drawing 4 (a), (b), and (c), 1 is a rectangle-like insulating substrate, and by notching 2, the individual electrodes T1-T10 form between each in both ends so that it may be isolated -- having -- **** -- one side -- T1-T5 -- T6-T10 are already prepared in one side. Furthermore, T1 and T6 which are formed in ends among the individual electrodes T1-T10, and face each other on the diagonal line are an electrical-potential-difference terminal, and an electrical potential difference is impressed to two electrodes. Other individual electrodes T2-T5, and T7-T10 are resistance terminals, and they are connected to the resistance element 3, respectively. It connects electrically, respectively, and the individual electrode which faces each other among the individual electrodes T1-T10 is prepared in the shape of a straight line so that the common electrode 4 may straddle these five connected electrically. At this time, about three of a center, it straddles so that one resistance element 3 may be formed at a time in one side of the common electrode 4, and between a resistance element 3 and electrical-potential-difference terminals is straddled about two of ends. 5 -- a protective coat -- it is -- at least -- a resistance element 3 -- all -- a wrap -- it is formed like. In addition, the front face has exposed the individual electrodes T1-T10, respectively, without covering the part with a protective coat 5 at least.
[0006] Moreover, generally a chip form resister network is prepared between ICs, impresses the electrical potential difference inputted into wiring between ICs from the electrical-potential-difference terminal through a resistance element 3, and it is used in order to pull up the electrical potential difference of wiring between ICs.
[0007]
[Problem(s) to be Solved by the Invention] The conventional chip form resister network constituted as mentioned above has variation in the die length of the common electrode section from a part for the connection of each resistance element and a common electrode to an electrical-potential-difference terminal. Moreover, when using it in a RF circuit, generally the inductance component between the resistance terminal with which an electrode has an inductance component proportional to the die length, and a common electrode section becomes long, and an electrical-potential-difference terminal has a wiring part larger than the inductance component between the resistance terminal which becomes short, and an electrical-potential-

difference terminal. Therefore, since it varied with the inductance component between each resistance terminal and an electrical-potential-difference terminal when using the conventional chip form resister network in a RF circuit, the RF signal deformed and components, a set, etc. incorporating the conventional chip form resister network had a technical problem called a lifting and a cone in malfunction.

[0008] This invention solves the above-mentioned conventional technical problem, and even if used in a high frequency circuit, it aims to let the components incorporating a chip form resister network, a set, etc. provide a lifting with a pile chip form resister network for malfunction.

[0009]

[Means for Solving the Problem] In order to attain the above-mentioned object the chip form resister network of this invention A rectangle-like insulating substrate and two or more individual electrodes prepared in the edge of this insulating substrate, Two or more resistance elements prepared so that it might be joined to said individual electrode, and the common electrode prepared so that it might be joined to said resistance element and electric target, It is what was constituted from a bump electrode prepared in parts other than near the ends near the ends of this common electrode. Since all individual electrodes become a resistance terminal and the bump electrode prepared in parts other than near the ends near the ends of a common electrode becomes an electrical-potential-difference terminal by this, Die length between each resistance terminal and an electrical-potential-difference terminal and its variation are made small, and can also make small the inductance component between each resistance terminal and an electrical-potential-difference terminal, and its variation. Therefore, the inductance component between each resistance terminal and an electrical-potential-difference terminal and its variation can be made small, and even if used in a high frequency circuit, a pile chip form resister network is obtained for components, a set, etc. incorporating a chip form resister network by the lifting in malfunction.

[0010]

[Embodiment of the Invention] Two or more individual electrodes with which invention of this invention according to claim 1 was prepared in the rectangle-like insulating substrate and the edge of this insulating substrate, Two or more resistance elements prepared so that it might be joined to said individual electrode, and the common electrode prepared so that it might be joined to said resistance element and electric target, It is what consists of a bump electrode prepared in parts other than near the ends near the ends of this common electrode. Since according to this configuration all individual electrodes become a resistance terminal and the bump electrode prepared in parts other than near the ends near the ends of a common electrode serves as an electrical-potential-difference terminal, 1 more electrical-potential-difference terminal can be prepared at least among these near the ends of a common electrode. Therefore, since die length between each resistance terminal and an electrical-potential-difference terminal and its variation can be made small, it has an operation that the inductance component between each resistance terminal and an electrical-potential-difference terminal and its variation can be made small.

[0011] Furthermore, since it is not necessary to form solder in a side face and since surface mounting of this chip form resister network is carried out to a mounting substrate with a bump electrode, and it is not necessary to prepare an electrical-potential-difference terminal in the edge of a substrate, the number of the individual electrodes of a substrate edge becomes fewer. Therefore, a component-side product has an operation that become small and high density assembly becomes possible.

[0012] Invention according to claim 2 is what prepared the bump electrode in all the junctions of a common electrode and a resistance element. Since according to this configuration all individual electrodes become a resistance terminal and the bump electrode prepared in all the junctions of a common electrode and a resistance element serves as an electrical-potential-difference terminal, A common electrode stops existing between each resistance terminal and an electrical-potential-difference terminal, and the variation can be abolished mostly by this smallest [die length / between each resistance terminal and an electrical-potential-difference terminal]. It has an operation that the variation can be abolished mostly smallest [component / between

each resistance terminal and an electrical-potential-difference terminal / inductance].
[0013] Furthermore, since it is not necessary to form solder in a side face and since surface mounting of this chip form resister network is carried out to a mounting substrate with a bump electrode, and it is not necessary to prepare an electrical-potential-difference terminal in the edge of a substrate, the number of the individual electrodes of a substrate edge becomes fewer. Therefore, a component-side product has an operation that become small and high density assembly becomes possible.
[0014] Invention according to claim 3 to the both ends of a rectangle-like insulating substrate and this insulating substrate, respectively The individual electrode of same number **********, Two or more resistance elements prepared so that two individual electrodes which face each other might be joined, respectively, It is what consists of a common electrode prepared so that it might be joined to said all resistance elements and electric targets ranging over all these resistance elements, and a bump electrode prepared in all the junctions of said common electrode and resistance element. According to this configuration, all individual electrodes become a resistance terminal, and it is prepared so that two individual electrodes which a resistance element faces may be joined, respectively. And the bump electrode which was formed so that a common electrode might straddle all these resistance elements, and so that it might be joined to said all resistance elements and electric targets, and was prepared in all the junctions of a common electrode and a resistance element serves as an electrical-potential-difference terminal. Since a common electrode stops existing between each resistance terminal and an electrical-potential-difference terminal by this, the variation can be abolished mostly smallest [die length / between each resistance terminal and an electrical-potential-difference terminal], and the inductance component between each resistance terminal and an electrical-potential-difference terminal can abolish the variation mostly smallest. Moreover, in order for what is necessary to be just to prepare one bump electrode to two resistance terminals which face each other, there are few bump electrodes, it ends and it has an operation that the yield in production becomes good.
[0015] Furthermore, since it is not necessary to form solder in a side face and since surface mounting of this chip form resister network is carried out to a mounting substrate with a bump electrode, and it is not necessary to prepare an electrical-potential-difference terminal in the edge of a substrate, the number of the individual electrodes of a substrate edge becomes fewer. Therefore, a component-side product has an operation that become small and high density assembly becomes possible.
[0016] (Gestalt 1 of operation) The gestalt 1 of operation of this invention is explained hereafter, referring to a drawing.
[0017] The plan of a chip form resister network [in / in drawing 1 (a) / the gestalt 1 of operation of this invention] and drawing 1 (b) are these sectional views between B-B of drawing 1 (a).
[0018] In drawing 1 , 11 is a rectangle-like insulating substrate and consists of an alumina, glass, etc. 12 is a common electrode, along with the center line of the top face of an insulating substrate 11, it is prepared in the shape of a straight line, and nickel and a two-layer eye consist [the 1st layer] of copper. 13 is an individual electrode, is prepared four pieces [a total of eight] at a time in the both ends of the field in which the common electrode 12 was formed, respectively, and consists of the same ingredient as the common electrode 12. this individual electrode 13 -- all serve as a resistance terminal. 14 is a resistance element, it is formed so that it may be in the field in which the common electrode 12 was formed and two individual electrode 13 comrades which face each other may be joined, respectively, and it consists of nickel chromium, tantalum nitride, etc. It straddles, and it is prepared so that it may join to all the resistance elements 14 electrically, so that the common electrode 12 may divide all the resistance elements 14 into about two equally. 15 is a bump electrode, is prepared in all the junctions of the common electrode 12 and a resistance element 14, and individual electrodes 13, and consists of solder. The bump electrode 15 prepared in all the junctions of the common electrode 12 and a resistance element 14 serves as an electrical-potential-difference terminal, and a resistance element 14 and wiring between ICs are electrically joined with the bump

electrode 15 prepared in all the individual electrodes 13 of all, i.e., resistance terminals. 16 is a protective coat, and the part in which the resistance element 14 is formed in the method of a wrap and the bump electrode 15 at least is prepared so that the bump electrode 15 may be exposed, and it consists of the thermosetting resin ingredient of an ultraviolet curing form. Thus, by forming a protective coat 16, the long-term dependability of a resistance element 14 can be raised.

[0019] Drawing 2 is drawing showing the equal circuit of the chip form resister network in the gestalt 1 of operation of this invention. this chip form resister network -- between the electrode 13 according to each, and the common electrodes 12 -- a resistance element 14 -- the common electrode 12 -- about -- the resistance r1-r8 which divided equally two and was formed is accumulated, and four bump electrodes B1 - B4 form in all the junctions of the common electrode 12 and a resistance element 14 -- having -- further -- the individual electrode 13 -- eight bump electrode B5-B12 will be formed in all.

[0020] By the above-mentioned configuration, since the common electrode 12 stops existing between each resistance terminal and an electrical-potential-difference terminal, the variation can be abolished mostly smallest [die length / between each resistance terminal and an electrical-potential-difference terminal], and the variation can be abolished mostly smallest [component / between each resistance terminal and an electrical-potential-difference terminal / inductance]. Moreover, in order for what is necessary to be just to form one bump electrode 15 to two resistance terminals which face each other, there are few bump electrodes 15, it ends and the yield in production becomes good. Therefore, even if used in a high frequency circuit, components, a set, etc. incorporating a chip form resister network cannot cause malfunction easily, and the effectiveness that the yield in production becomes good is acquired.

[0021] Furthermore, since it is not necessary to form solder in a side face and since surface mounting of this chip form resister network is carried out to a mounting substrate with the bump electrode 15, and it is not necessary to prepare an electrical-potential-difference terminal in the edge of a substrate, the number of the individual electrodes 13 of a substrate edge decreases to eight pieces from ten pieces to the conventional chip form resister network. Therefore, the effectiveness that a component-side product becomes small and the high density assembly of it becomes possible is also acquired.

[0022] About the chip form resister network in the gestalt 1 of operation of this invention constituted as mentioned above, the manufacture approach is explained below, referring to a drawing.

[0023] Drawing 3 is process drawing showing the manufacture approach of the chip form resister network in the gestalt 1 of operation of this invention.

[0024] First, as shown in drawing 3 (a), on an insulating substrate 11, film deposition of the nickel chromium is carried out by sputtering, with a photolithography method of construction, pattern formation is carried out and a resistance element 14 is formed.

[0025] Next, as shown in drawing 3 (b), film deposition of nickel and the copper is carried out by sputtering, with a photolithography method of construction, pattern formation is carried out and the common electrode 12 and the individual electrode 13 are formed simultaneously.

[0026] Next, as shown in drawing 3 (c), whole surface film deposition is carried out with a spin coat, pattern formation is carried out with a photolithography method of construction, and the protective coat 16 which has opening 17 in the location which forms the bump electrode 15 is formed.

[0027] Finally, as shown in drawing 3 (d), the bump electrode 15 is formed because supply soldering paste on an insulating substrate 11 by screen-stencil and it carries out a reflow, and the chip form resister network of this invention is formed.

[0028] In addition, although the example constituted from two-layer [of nickel/copper] explained the common electrode 12 and the individual electrode 13 in the above-mentioned explanation, you may constitute from other low electrical resistance materials, such as chromium/copper, and silver, and film deposition only of the predetermined section may be carried out by sputtering using approaches other than the photolithography method of construction also explaining the manufacture approach, for example, screen printing, and the

metal mask which prepared opening.
[0029] Moreover, although the example constituted from nickel chromium explained the resistance element 14, you may constitute from ingredients, such as ruthenium oxide and a tungsten, and film deposition only of the predetermined section may be carried out by sputtering using approaches other than the photolithography method of construction also explaining the manufacture approach, for example, screen printing, and the metal mask which prepared opening.

[0030] Moreover, although the example constituted from solder explained the bump electrode 15, you may constitute from other low-melt point point metals and conductive resin, and may carry out by approaches other than the screen-stencil also explaining the manufacture approach, for example, plating and the solder ball transferring method.
[0031] Moreover, although the example constituted from thermosetting resin of an ultraviolet curing form explained the protective coat (insulating layer) 16, film deposition only of the predetermined section may be carried out by sputtering using approaches other than the photolithography method of construction also explaining the manufacture approach, for example, screen printing, and the metal mask which prepared opening that what is necessary is just to constitute from an ingredient which is not damp into the ingredient of the bump electrodes 15, such as thermosetting resin and glass.
[0032] In addition, [whether it constitutes so that not only the resistance element 14 but the common electrode 12 may exist between two individual electrode 13 which face each other in addition to the above-mentioned configuration, and] Even if it forms the individual electrode 13 in one side instead of ends of an insulating substrate 11 and forms the bump electrode 15 in all the junctions of the common electrode 12 and a resistance element 14 Even if used by the same reason as the above in a high frequency circuit, components, a set, etc. incorporating a chip form resister network do not cause malfunction, but the effectiveness whose high density assembly becomes possible is also acquired according to it.
[0033] moreover , since die length between each resistance terminal and an electrical potential difference terminal and its variation can make small even if it prepare the location of the bump electrode 15 establish in the common electrode 12 in two places and the medium of those near the ends of the common electrode 12 , the inductance component between each resistance terminal and an electrical potential difference terminal and its variation can make small , and even if use in a high frequency circuit , the effectiveness of a pile in components , a set , etc. incorporating a chip form resister network be acquire by the lifting in malfunction . Furthermore, since it is not necessary to form solder in a side face and since surface mounting of this chip form resister network is carried out to a mounting substrate with the bump electrode 15, and it is not necessary to prepare an electrical-potential-difference terminal in the edge of a substrate, the number of individual electrodes becomes fewer. Therefore, the effectiveness that a component-side product becomes small and the high density assembly of it becomes possible is also acquired.
[0034] Moreover, although the bump electrode 15 is formed in the individual electrode 13, since it is uninfluential to the die length between the electrode 13 (resistance terminal) according to each, and an electrical-potential-difference terminal even if it attaches the individual electrode 13 in a mounting substrate except bump electrode 15, the same effectiveness is acquired.
[0035]
[Effect of the Invention] Two or more individual electrodes which were prepared in the rectangle-like insulating substrate and the edge of this insulating substrate as mentioned above according to this invention, Two or more resistance elements prepared so that it might be joined to said individual electrode, and the common electrode prepared so that it might be joined to said resistance element and electric target, It is what consists of a bump electrode prepared in parts other than near the ends near the ends of this common electrode. Since according to this configuration all individual electrodes become a resistance terminal and the bump electrode prepared in parts other than near the ends near the ends of a common electrode serves as an electrical-potential-difference terminal, 1 more electrical-potential-difference terminal can be prepared at least among these near the ends of a common electrode. Therefore, components, a

set, etc. which incorporated the chip form resister network even if it could make small the inductance component between each resistance terminal and an electrical-potential-difference terminal and its variation and was used in the high frequency circuit since die length between the electrode according to each and an electrical-potential-difference terminal and its variation were made small are a pile to a lifting about malfunction. Furthermore, since the number of individual electrodes becomes fewer since it is not necessary to form solder in a side face and since surface mounting of this chip form resister network is carried out to a mounting substrate with a bump electrode, and it is not necessary to prepare an electrical-potential-difference terminal in the edge of a substrate, and a component-side product becomes small by this, the advantageous effectiveness that the chip form resister network where high density assembly becomes possible is obtained is acquired.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

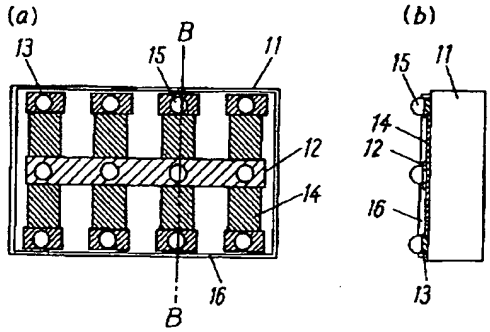
[Brief Description of the Drawings]
[Drawing 1] (a) The plan of the chip form resister network in the gestalt 1 of operation of this invention
(b) The sectional view between these B-B
[Drawing 2] Drawing showing the equal circuit of the chip form resister network in the gestalt 1 of operation of this invention
[Drawing 3] Process drawing showing the manufacture approach of the chip form resister network in the gestalt 1 of operation of this invention
[Drawing 4] (a) The plan of the conventional chip form resister network
(b) The sectional view between these A-A
(c) Drawing showing this equal circuit
[Description of Notations]
11 Insulating Substrate
12 Common Electrode
13 Individual Electrode
14 Resistance Element
15 Bump Electrode
16 Protective Coat

[Translation done.]

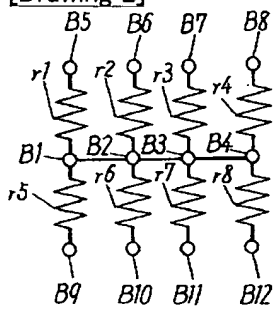
DRAWINGS

[Drawing 1]

11 絶縁基板
12 共通電極
13 個別電極
14 抵抗素子
15 バンプ電極
16 保護膜



[Drawing 2]



[Drawing 3]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号
特開2000－77218
(P2000－77218A)
(43)公開日　平成12年３月14日(2000.3.14)

(51)Int.Cl.⁷	識別記号	ＦＩ	テーマコード（参考）
Ｈ０１Ｃ　13/02		Ｈ０１Ｃ　13/02	Ｂ

審査請求　未請求　請求項の数３　ＯＬ　（全 6 頁）

(21)出願番号　特願平10－246781

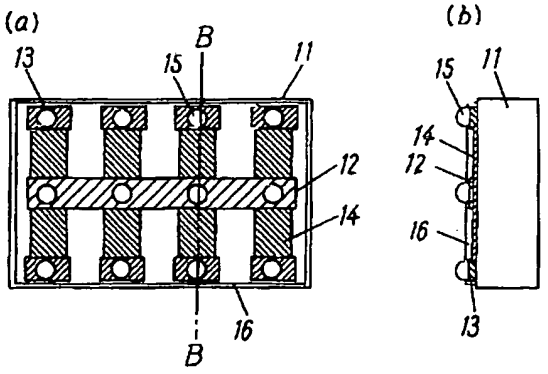
(22)出願日　平成10年９月１日(1998.9.1)

(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地
(72)発明者　木下　泰治
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(72)発明者　渋谷　直樹
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(72)発明者　星徳　聖治
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(74)代理人　100097445
弁理士　岩橋　文雄　（外２名）

(54)【発明の名称】　チップ形抵抗ネットワーク

(57)【要約】
【課題】　高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしにくいチップ形抵抗ネットワークを提供することを目的とする。
【解決手段】　矩形状の絶縁基板１１と、この絶縁基板１１の端部に設けられた複数の個別電極１３と、個別電極１３と接合されるように設けられた複数の抵抗素子１４と、抵抗素子１４と電気的に接合されるように設けられた共通電極１２と、共通電極１２の両端近傍および両端近傍以外の部分に設けられたバンプ電極１５とで構成する。

11 絶縁基板
12 共通電極
13 個別電極
14 抵抗素子
15 バンプ電極
16 保護膜



【特許請求の範囲】
【請求項1】 矩形状の絶縁基板と、この絶縁基板の端部に設けられた複数の個別電極と、前記個別電極と接合されるように設けられた複数の抵抗素子と、前記抵抗素子と電気的に接合されるように設けられた共通電極と、この共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極とからなるチップ形抵抗ネットワーク。
【請求項2】 バンプ電極を、共通電極と抵抗素子との全ての接合点に設けた請求項1記載のチップ形抵抗ネットワーク。
【請求項3】 矩形状の絶縁基板と、この絶縁基板の両端部にそれぞれ同数設けられた複数の個別電極と、向かい合う2つの個別電極同士をそれぞれ接合するように設けられた複数の抵抗素子と、この全ての抵抗素子を跨ぎ且つ全ての前記抵抗素子と電気的に接合されるように設けられた共通電極と、前記共通電極と抵抗素子との全ての接合点に設けられたバンプ電極とからなるチップ形抵抗ネットワーク。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本発明は、共通電極を有するチップ形抵抗ネットワークに関するものである。
【0002】
【従来の技術】従来のこの種のチップ形抵抗ネットワークとしては、特開平5-33517号公報に記載されたものが知られている。
【0003】以下、従来のチップ形抵抗ネットワークについて、図面を参照しながら説明する。
【0004】図4(a)は従来のチップ形抵抗ネットワークの上面図、図4(b)は図4(a)のA-A間における同断面図、図4(c)は同等価回路を示す図である。
【0005】図4(a)、(b)、(c)において、1は矩形状の絶縁基板で、両端部に切り欠き2によって、それぞれの間を隔離されるよう個別電極T1～T10が形成されており、片側にT1～T5、もう片側にはT6～T10が設けられている。さらに、個別電極T1～T10のうち、両端に形成され且つ対角線上に向かい合っているT1およびT6は電圧端子であり、両電極に電圧が印加される。他の個別電極T2～T5およびT7～T10は抵抗端子であり、それぞれ抵抗素子3に接続されている。個別電極T1～T10のうち向かい合う個別電極はそれぞれ電気的に接続され、共通電極4がこの電気的に接続された5本を跨ぐように直線状に設けられている。このとき中央の3本については、共通電極4の片側に抵抗素子3が1個ずつ設けられるように跨ぎ、且つ両端の2本については、抵抗素子3と電圧端子の間を跨ぐ。5は保護膜で、少なくとも抵抗素子3全てを覆うように形成されている。なお、個別電極T1～T10はそれぞれ表面の少なくともその一部が保護膜5に覆われずに露出している。
【0006】また、チップ形抵抗ネットワークは一般にICとICの間に設けられ、ICとIC間の配線に、電圧端子より入力された電圧を、抵抗素子3を介して印加し、ICとIC間の配線の電圧を引き上げる目的で使用される。
【0007】
【発明が解決しようとする課題】以上のように構成された従来のチップ形抵抗ネットワークは、各抵抗素子と共通電極との接続部分から、電圧端子までの共通電極部分の長さにバラツキがある。また、高周波回路で使用するとき、一般に電極はその長さに比例したインダクタンス成分を持ち、共通電極部分が長くなる抵抗端子と電圧端子間のインダクタンス成分は、配線部分が短くなる抵抗端子と電圧端子間のインダクタンス成分よりも大きい。従って、従来のチップ形抵抗ネットワークを高周波回路で使用する時、各抵抗端子と電圧端子間のインダクタンス成分を持ち且つばらつくため、高周波信号が変形し、従来のチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしやすいという課題を有していた。
【0008】本発明は、上記従来の課題を解決するもので、高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしにくいチップ形抵抗ネットワークを提供することを目的とする。
【0009】
【課題を解決するための手段】上記目的を達成するために本発明のチップ形抵抗ネットワークは、矩形状の絶縁基板と、この絶縁基板の端部に設けられた複数の個別電極と、前記個別電極と接合されるように設けられた複数の抵抗素子と、前記抵抗素子と電気的に接合されるように設けられた共通電極と、この共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極とで構成したもので、これにより、個別電極全てが抵抗端子になり、且つ共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極が電圧端子になるため、各抵抗端子と電圧端子間の長さおよびそのバラツキが小さくでき、各抵抗端子と電圧端子間のインダクタンス成分およびそのバラツキも小さくできる。従って、各抵抗端子と電圧端子間のインダクタンス成分およびそのバラツキを小さくでき、高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしにくいチップ形抵抗ネットワークが得られる。
【0010】
【発明の実施の形態】本発明の請求項1に記載の発明は、矩形状の絶縁基板と、この絶縁基板の端部に設けられた複数の個別電極と、前記個別電極と接合されるように設けられた複数の抵抗素子と、前記抵抗素子と電気的

に接合されるように設けられた共通電極と、この共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極とからなるもので、この構成によれば、個別電極全てが抵抗端子になり、且つ共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極が電圧端子となるため、共通電極の両端近傍および、これらの間に少なくともう1つ電圧端子を設けることができる。従って、各抵抗端子と電圧端子間の長さおよびそのバラツキを小さくできるため、各抵抗端子と電圧端子間のインダクタンス成分およびそのバラツキを小さくできるという作用を有するものである。

【0011】さらに、バンプ電極によってこのチップ形抵抗ネットワークが実装基板に面実装されるため側面にはんだを形成しなくて済み、また基板の端部に電圧端子を設けなくて済むため基板端部の個別電極の数が減る。従って、実装面積が小さくなり、高密度実装が可能になるという作用を有するものである。

【0012】請求項2に記載の発明は、バンプ電極を、共通電極と抵抗素子との全ての接合点に設けたもので、この構成によれば、個別電極全てが抵抗端子になり、且つ共通電極と抵抗素子との接合点の全てに設けられたバンプ電極が電圧端子となるため、各抵抗端子と電圧端子間には共通電極が存在しなくなり、これにより各抵抗端子と電圧端子間の長さを最も小さく且つそのバラツキをほぼなくすことができ、各抵抗端子と電圧端子間のインダクタンス成分を最も小さく且つそのバラツキをほぼなくすことができるという作用を有するものである。

【0013】さらに、バンプ電極によってこのチップ形抵抗ネットワークが実装基板に面実装されるため側面にはんだを形成しなくて済み、また基板の端部に電圧端子を設けなくて済むため基板端部の個別電極の数が減る。従って、実装面積が小さくなり、高密度実装が可能になるという作用を有するものである。

【0014】請求項3に記載の発明は、矩形状の絶縁基板と、この絶縁基板の両端部にそれぞれ同数設けられた複数の個別電極と、向かい合う2つの個別電極同士をそれぞれ接合するように設けられた複数の抵抗素子と、この全ての抵抗素子を跨ぎ且つ全ての前記抵抗素子と電気的に接合されるように設けられた共通電極と、前記共通電極と抵抗素子との全ての接合点に設けられたバンプ電極とからなるもので、この構成によれば、個別電極全てが抵抗端子になり、また抵抗素子が向かい合う2つの個別電極同士をそれぞれ接合されるよう設けられ、且つ共通電極がこの全ての抵抗素子を跨ぐように且つ全ての前記抵抗素子と電気的に接合されるように形成され、また共通電極と抵抗素子との接合点の全てに設けられたバンプ電極が電圧端子となる。これにより各抵抗端子と電圧端子間に共通電極が存在しなくなるため、各抵抗端子と電圧端子間の長さを最も小さく且つそのバラツキをほぼなくすことができ、各抵抗端子と電圧端子間のインダクタンス成分が最も小さく且つそのバラツキをほぼなくすことができる。また、向かい合う2つの抵抗端子に対して、バンプ電極を1つ設ければ良いことになるため、バンプ電極の数が少なくて済み、生産での歩留まりが良くなるという作用を有するものである。

【0015】さらに、バンプ電極によってこのチップ形抵抗ネットワークが実装基板に面実装されるため側面にはんだを形成しなくて済み、また基板の端部に電圧端子を設けなくて済むため基板端部の個別電極の数が減る。従って、実装面積が小さくなり、高密度実装が可能になるという作用を有するものである。

【0016】(実施の形態1)以下、本発明の実施の形態1について、図面を参照しながら説明する。

【0017】図1(a)は、本発明の実施の形態1におけるチップ形抵抗ネットワークの上面図、図1(b)は図1(a)のB-B間における同断面図である。

【0018】図1において、11は矩形状の絶縁基板で、アルミナやガラスなどから成る。12は共通電極で、絶縁基板11の上面の中心線に沿って直線状に設けられ、1層目がニッケル、2層目が銅から成る。13は個別電極で、共通電極12が設けられた面の両端部にそれぞれ4個ずつ計8個設けられ、共通電極12と同一材料から成る。この個別電極13全てが抵抗端子となる。14は抵抗素子で、共通電極12が設けられた面にあり、向かい合う2つの個別電極13同士をそれぞれ接合するよう形成され、ニッケルクロムや窒化タンタルなどから成る。共通電極12が全ての抵抗素子14をほぼ2等分するように跨ぎ、且つ全ての抵抗素子14と電気的に接合するように設けられている。15はバンプ電極で、共通電極12と抵抗素子14との接合点および個別電極13の全てに設けられ、はんだから成る。共通電極12と抵抗素子14との接合点全てに設けられたバンプ電極15が電圧端子となり、個別電極13の全て、すなわち抵抗端子全てに設けられたバンプ電極15によって、抵抗素子14とICとICの間の配線とが電気的に接合される。16は保護膜で、少なくとも抵抗素子14を覆うよう且つバンプ電極15が設けられている部分はバンプ電極15が露出するように設けられ、紫外線硬化形の熱硬化性樹脂材料から成る。このように保護膜16を設けることで、抵抗素子14の長期信頼性を向上させることができる。

【0019】図2は本発明の実施の形態1におけるチップ形抵抗ネットワークの等価回路を示す図である。このチップ形抵抗ネットワークは、各個別電極13と共通電極12の間に、抵抗素子14を共通電極12によってほぼ2等分して形成された抵抗r1～r8を集積し、共通電極12と抵抗素子14との接合点全てに4個のバンプ電極B1～B4が形成され、さらに個別電極13全てに8個のバンプ電極B5～B12が形成されていることになる。

【００２０】上記構成により、各抵抗端子と電圧端子間に共通電極１２が存在しなくなるため、各抵抗端子と電圧端子間の長さを最も小さく且つそのバラツキをほぼなくすことができ、各抵抗端子と電圧端子間のインダクタンス成分を最も小さく且つそのバラツキをほぼなくすことができる。また、向かい合う２つの抵抗端子に対して、バンプ電極１５を１つ設ければよいことになるため、バンプ電極１５の数が少なくて済み、生産での歩留まりが良くなる。従って高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしにくく、また生産での歩留まりが良くなるという効果が得られる。

【００２１】さらに、バンプ電極１５によってこのチップ形抵抗ネットワークが実装基板に面実装されるため、側面にはんだを形成しなくて済み、また基板の端部に電圧端子を設けなくて済むため、従来のチップ形抵抗ネットワークに対して基板端部の個別電極１３の数が１０個から８個に減る。従って、実装面積が小さくなり、高密度実装が可能となる効果も得られる。

【００２２】以上のように構成された本発明の実施の形態１におけるチップ形抵抗ネットワークについて、以下にその製造方法を図面を参照しながら説明する。

【００２３】図３は本発明の実施の形態１におけるチップ形抵抗ネットワークの製造方法を示す工程図である。

【００２４】まず、図３（ａ）に示すように、絶縁基板１１上にニッケルクロムをスパッタリングにより着膜し、フォトリソグラフィ工法によってパターン形成して抵抗素子１４を形成する。

【００２５】次に、図３（ｂ）に示すように、ニッケルと銅をスパッタリングにより着膜し、フォトリソグラフィ工法によってパターン形成して、共通電極１２と個別電極１３を同時に形成する。

【００２６】次に、図３（ｃ）に示すように、スピンコートにより全面着膜してフォトリソグラフィ工法によってパターン形成して、バンプ電極１５を形成する位置に開口部１７を持つ保護膜１６を形成する。

【００２７】最後に、図３（ｄ）に示すように、はんだペーストをスクリーン印刷により絶縁基板１１上に供給し、リフローすることでバンプ電極１５を形成して、本発明のチップ形抵抗ネットワークを形成するものである。

【００２８】なお、上記の説明では、共通電極１２、個別電極１３をニッケル／銅の２層で構成した例で説明したが、クロム／銅、銀等の他の低抵抗材料で構成しても良く、その製造方法についても説明したフォトリソグラフィ工法以外の方法、例えばスクリーン印刷法や、開口部を設けたメタルマスクを用いスパッタリングにより所定部のみ着膜しても良い。

【００２９】また、抵抗素子１４をニッケルクロムで構成した例で説明したが、酸化ルテニウム、タングステン等の材料で構成しても良く、その製造方法についても説明したフォトリソグラフィ工法以外の方法、例えばスクリーン印刷法や、開口部を設けたメタルマスクを用いスパッタリングにより所定部のみ着膜しても良い。

【００３０】また、バンプ電極１５をはんだで構成した例で説明したが、他の低融点金属や導電性樹脂で構成しても良く、その製造方法についても説明したスクリーン印刷以外の方法、例えばめっきやはんだボール移載法で行っても良い。

【００３１】また、保護膜（絶縁層）１６を紫外線硬化形の熱硬化性樹脂で構成した例で説明したが、熱硬化性樹脂やガラス等のバンプ電極１５の材料に濡れない材料で構成すれば良く、その製造方法についても説明したフォトリソグラフィ工法以外の方法、例えばスクリーン印刷法や、開口部を設けたメタルマスクを用いスパッタリングにより所定部のみ着膜しても良い。

【００３２】なお、上記構成以外に、向かい合う２つの個別電極１３同士間に抵抗素子１４だけでなく共通電極１２も存在するよう構成するか、個別電極１３を絶縁基板１１の両端ではなく片側に設け、且つ共通電極１２と抵抗素子１４の接合点全てにバンプ電極１５を設けても、上記と同じ理由によって、高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こさず、高密度実装が可能となる効果も得られる。

【００３３】また、共通電極１２に設けられるバンプ電極１５の位置を、共通電極１２の両端近傍の２ヵ所およびその中間に設けても、各抵抗端子と電圧端子間の長さ且つそのバラツキを小さくできるため、各抵抗端子と電圧端子間のインダクタンス成分且つそのバラツキを小さくでき、高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしにくいという効果が得られる。さらに、バンプ電極１５によってこのチップ形抵抗ネットワークが実装基板に面実装されるため、側面にはんだを形成しなくて済み、また基板の端部に電圧端子を設けなくて済むため個別電極の数が減る。従って、実装面積が小さくなり、高密度実装が可能となる効果も得られる。

【００３４】また、個別電極１３にバンプ電極１５を設けるとしたが、バンプ電極１５以外で個別電極１３を実装基板に取り付けても、各個別電極１３（抵抗端子）と電圧端子間の長さに影響はないので、同じ効果が得られる。

【００３５】

【発明の効果】以上のように本発明によれば、矩形状の絶縁基板と、この絶縁基板の端部に設けられた複数の個別電極と、前記個別電極と接合されるように設けられた複数の抵抗素子と、前記抵抗素子と電気的に接合されるように設けられた共通電極と、この共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極とか

らなるもので、この構成によれば、個別電極全てが抵抗端子になり、且つ共通電極の両端近傍および両端近傍以外の部分に設けられたバンプ電極が電圧端子となるため、共通電極の両端近傍および、これらの間に少なくともう1つ電圧端子を設けることができる。従って各個別電極と電圧端子間の長さおよびそのバラツキを小さくできるため、各抵抗端子と電圧端子間のインダクタンス成分およびそのバラツキを小さくでき、高周波回路で使用されてもチップ形抵抗ネットワークを組み込んだ部品やセットなどが誤動作を起こしにくい。さらに、バンプ電極によってこのチップ形抵抗ネットワークが実装基板に面実装されるため側面にはんだを形成しなくて済み、また基板の端部に電圧端子を設けなくて済むため個別電極の数が減り、これにより実装面積が小さくなるため、高密度実装が可能になるチップ形抵抗ネットワークが得られるという有利な効果が得られる。

【図面の簡単な説明】

【図1】(a)本発明の実施の形態1におけるチップ形抵抗ネットワークの上面図

(b)同B－B間における断面図

【図2】本発明の実施の形態1におけるチップ形抵抗ネットワークの等価回路を示す図

【図3】本発明の実施の形態1におけるチップ形抵抗ネットワークの製造方法を示す工程図

【図4】(a)従来のチップ形抵抗ネットワークの上面図

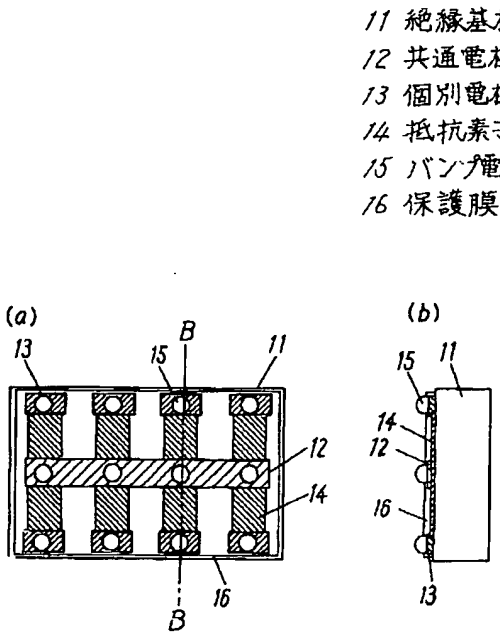
(b)同A－A間における断面図

(c)同等価回路を示す図

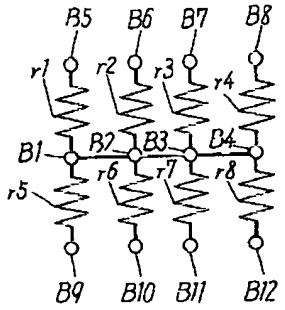
【符号の説明】

11　絶縁基板
12　共通電極
13　個別電極
14　抵抗素子
15　バンプ電極
16　保護膜

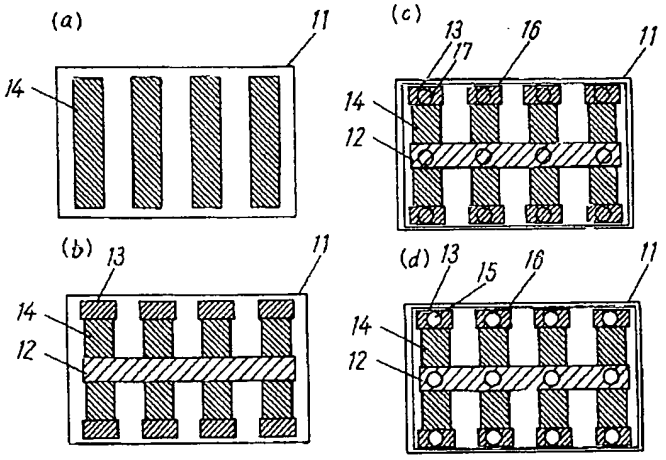
【図1】



【図2】



【図3】



11 絶縁基板
12 共通電極
13 個別電極
14 抵抗素子
15 バンプ電極
16 保護膜

【図4】